REMARKS

Claims 1, 2, 9, 11, 12 and 18 have been amended. Claims 1-9, 11-18, 20 and 21 are presently pending in the application.

The amendment filed February 22, 2005 was objected to under 35 U.S.C. 132(a) as allegedly introducing new matter into the disclosure, and claims 1-9 and 11-18 were rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the written description requirement. In particular, the Examiner stated that recitations of a second temperature coefficient being the same as a first temperature coefficient are not supported by the original disclosure. In response, Applicants direct the Examiner's attention to, for example, lines 20-22 on page 9 of Applicants' specification, which state:

> When the components of M1 and M6 are set to have the same or about the same temperature coefficients (e.g., all positive or all negative), then when IA increases IM6 increases also, and vice versa. This behavior can facilitate a stabilization of IR2 and VREF.

Furthermore, Applicants direct the Examiner's attention to, for example, page 7, line 20 to page 8, line 14 of Applicants' specification, which state:

> The current source transistor M1 is a PMOS transistor, and consequently may be expected to have a positive temperature coefficient. As temperature increases, current IA through the current source transistor M1 may be expected to increase. The increase in current is mirrored into the second current path IC across the output current mirror formed by the current source transistor M1 and the output transistor M2, increasing the current through the parallel combination of the thermal coupling transistor M6 and the second resistor R2. Without temperature compensation, the output reference voltage would vary with VGS1, in accordance with the relationship:
>
> $VREF = VGS1*(R2/R1)$, or
> $\partial VREF / \partial T = (R2/R1)\ (\partial VGS1 / \partial T) > 0$, where T = temperature.

> The thermal coupling transistor-like element M6 provides the necessary thermal compensation to maintain the output reference voltage regardless of thermal variations in VGS1. The thermal coupling transistor-like element M6 is a PMOS transistor, and consequently may be expected to have a positive temperature coefficient. As temperature increases, current through the thermal coupling transistor-like element M6 may be expected to increase, shunting a greater current from the second resistor R2 and allowing the voltage across the second resistor R2 to remain constant despite a greater current through the first resistor R1. Similarly, as temperature decreases, current through the thermal coupling transistor-like element M6 may be expected to decrease, diverting a greater portion of the first current from the first resistor R1 into the second resistor R2 and (again) allowing the voltage across the second resistor R2 to remain constant despite a greater current through the first resistor R1. However, the increased current flow through the second resistor R2 will increase the voltage across the second resistor R2, thereby increasing current flow through the thermal coupling transistor M6 and offsetting the temperature-induced decrease of current through the thermal coupling transistor M6.

It is thus respectfully submitted that the amendment filed February 22, 2005 does not introduce new matter.

Regarding prior-art, the Office Action has maintained the rejection of claims 20 and 21 under 35 U.S.C. 102(b) as allegedly being anticipated by Houghton et al. (U.S. Patent No. 6,087,820). Applicants respectfully disagree with this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (*Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). Thus, for a rejection under 35 U.S.C. 102(b) to be proper, every limitation recited in each rejected claim, which is rejected as being anticipated by a prior-art reference, must be clearly disclosed in that single prior-art reference. In the instant case, Applicants respectfully submit that the cited Houghton et al. reference does not disclose each and every element that is recited in the rejected claims, and, therefore, the cited Houghton et al. reference does not anticipate any of the claims under 35 U.S.C. § 102(b).

Applying the above Federal Circuit standard, Houghton et al. does not discloses a reference voltage generator, including, among other things, "a first resistive element; a PMOS transistor coupled to apply a gate-source voltage difference on the first resistive element to generate a first current; a current mirror for mirroring the first current to generate a second current; a second resistive element coupled to be applied with the second current to thereby generate a reference voltage; and an NMOS transistor connected to the second resistive element in parallel for compensating a variation of the gate-source voltage difference," as recited in independent claim 20. For instance, Houghton et al. nowhere discloses a combination of elements as recited in claim 20 comprising, among other things, "a PMOS transistor coupled to apply a gate-source voltage difference on the first resistive element to generate a first current." Accordingly, independent claim 20, and claim 21 which depends therefrom, are not anticipated by Houghton et al.

Applicants respectfully request that the outstanding objection and rejections be reconsidered and withdrawn.

In view of the above, Applicants submit that the application is now in condition for allowance, and an early indication of the same is requested. The Examiner is invited to contact the undersigned with any questions.

Respectfully submitted,

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